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(54) **Variable capacitor**

(57) A variable capacitor comprising a semiconductive substrate 10 having one surface 3 for generation a depletion layer thereon, an opposite surface 15 substantially parallel with said one surface and a lateral surface A, a depletion layer *d* and a capacitance reading section 13 provided along the lateral surface A of the semiconductive substrate, permitting the depletion layer *d* to expand to reach the lateral surface A by reversely biasing the depletion layer control section 14/12, whereby reading capacitance variation from the capacitance reading section 13. The depletion layer *d* and capacitance reading section 13 can be defined by a P-N junction, a MIS arrangement of a Schottky barrier.

FIG. 2

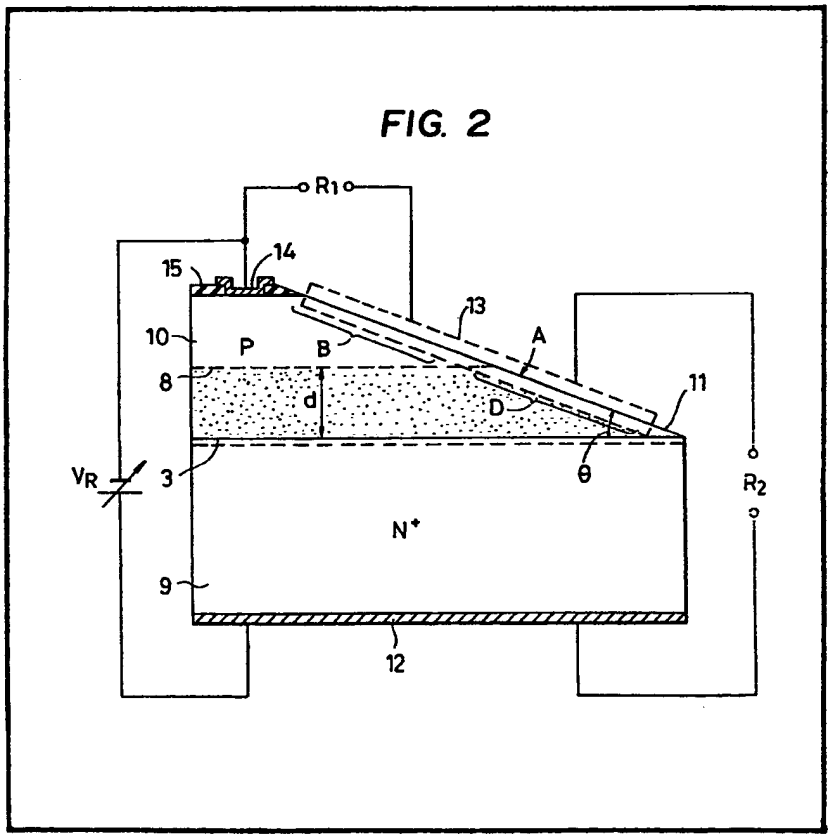

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FIG. 1
PRIOR ART

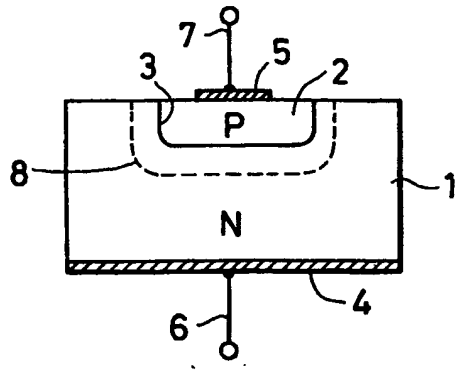


FIG. 2

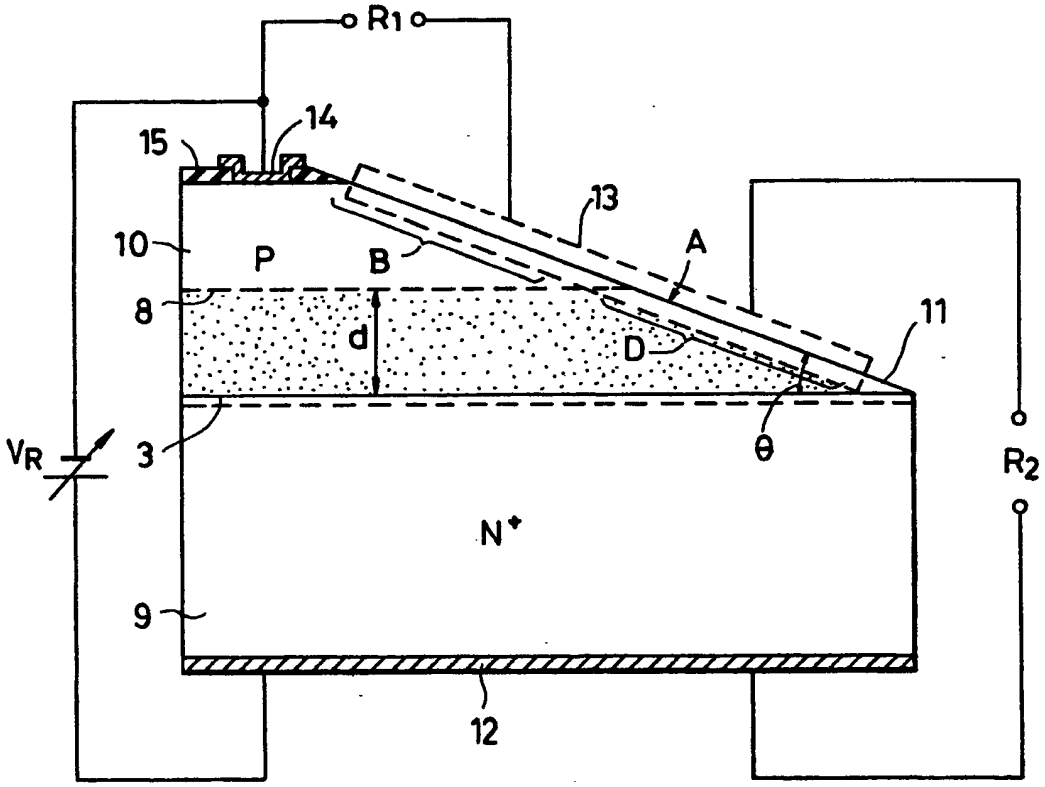


FIG. 3

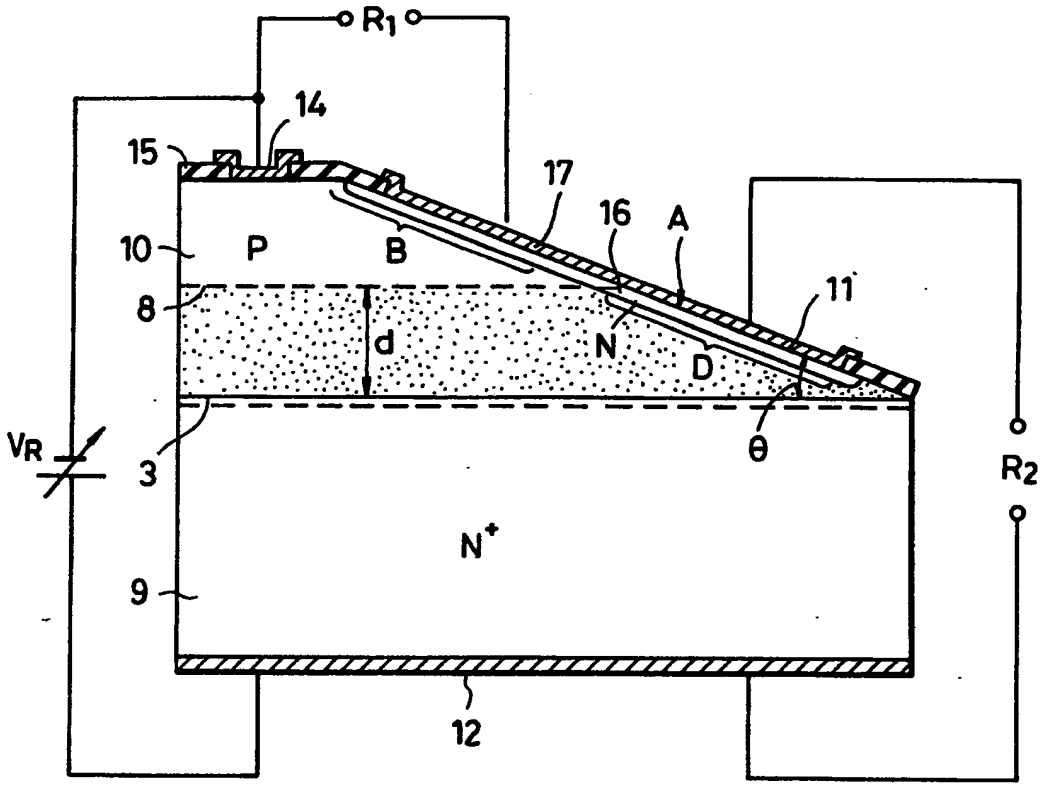


FIG. 4

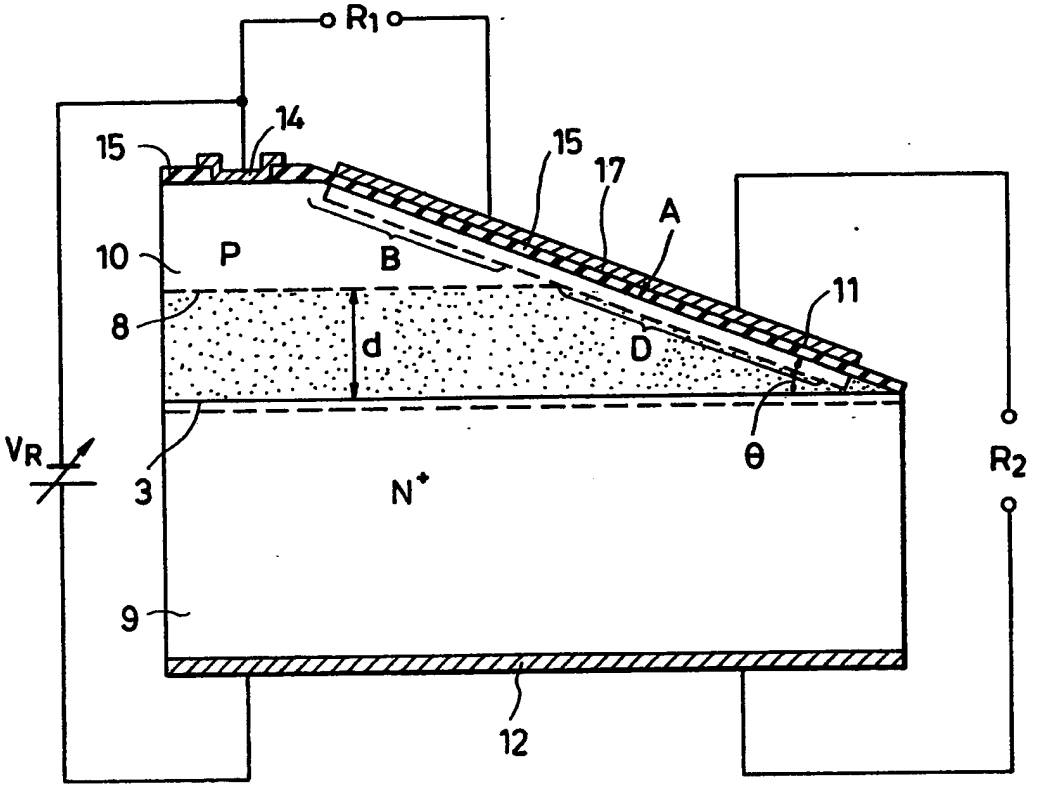
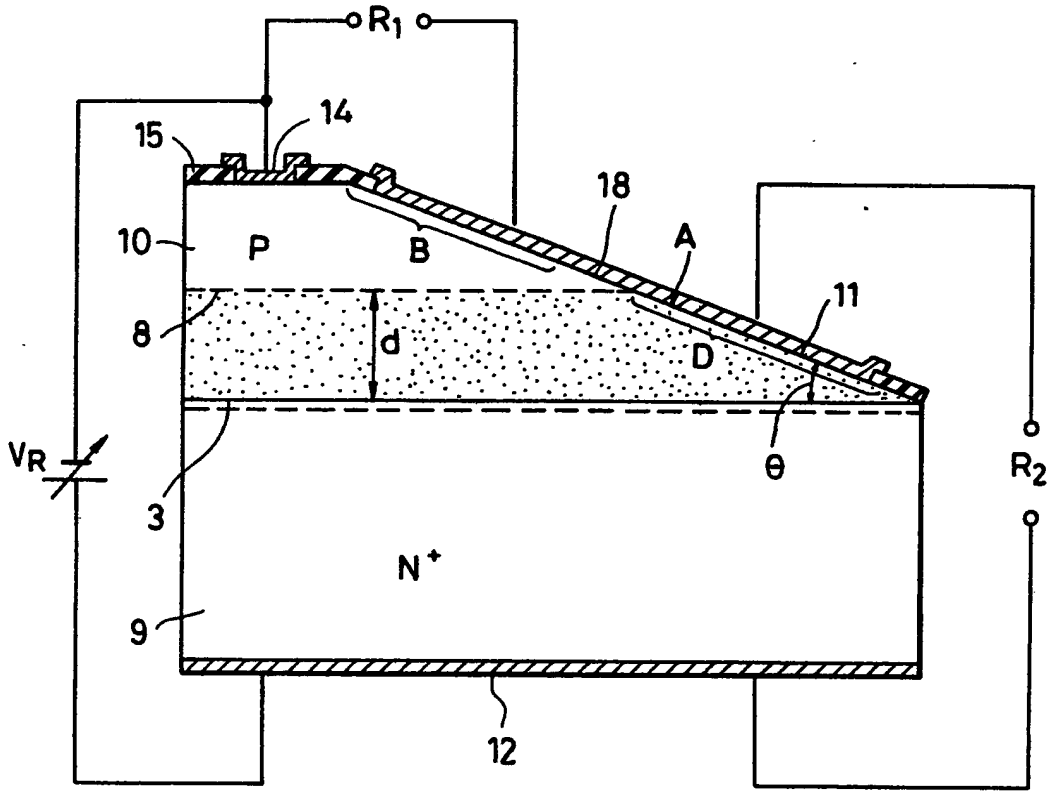


FIG. 5



SPECIFICATION
Variable capacitor

This invention relates to a variable capacitor having three terminals in which a capacitance reading section is provided on lateral surface of a semiconductive chip.

It is well known to utilize as variable capacitor a p-n junction element as shown in Figure 1. In this Figure, the reference numeral 1 denotes an n-type semiconductive layer; 2 is a p-type semiconductive region; 3 is a p—n junction; 4 and 5 are electrodes disposed in said layer 1 and region 2, respectively; 6 and 7 are outgoing or lead-out terminals disposed for said electrodes 4 and 5, respectively; and 8 is a depletion layer spreading from the p—n junction 3 and mainly on one side of the n-type layer 1 with low impurity concentration. In the above configuration of variable capacitor, the depletion layer 8 expands and contracts depending upon the bias voltage applied to said lead-out terminals 6 and 7, then change of capacitance due to the expansion or contraction of the depletion layer 8 being readable between the lead-out terminals 6 and 7.

However, the conventional or prior-art variable capacitors using the above-mentioned p—n junction elements represent the following disadvantages:

(1) Since the dependence upon the bias voltage of the depletion-layer capacitance in the p—n junction is utilized, the minimum capacitance depends upon the concentration of impurity in the semiconductive regions, while the maximum capacitance depends upon the increase of conductive component. Thus, it is practically impossible to provide a large change of the capacitance in a state where Q is large, and because of the change of Q being larger with the change of capacitance, a difficulty is experienced in the design of circuits.

(2) Because it is at the common lead-out terminal that the bias voltage is applied for change of the capacitance and that the change of the capacitance is read, when such prior-art variable capacitors are employed in resonance circuit or the like, input signal voltage itself will easily induce an unnecessary change of the capacitance, resulting in degradation of the signal. Further, since a special circuit configuration is needed for minimization of the interaction between the input signal voltage and bias voltage, such prior-art variable capacitors can be used only in a limited range of application.

(3) The concentration of impurity in the semiconductive regions is controlled by the diffusion method or ion-implantation method for determination of the depletion-layer capacitance; generally speaking, however, since such methods permit only a low available percentage, the conventional variable capacitors cannot practically be formed in integrated circuit.

Accordingly, the present invention seeks to overcome the above-mentioned drawbacks of the conventional field of technique concerning variable capacitors, by providing a variable capacitor in which capacitance reading section is provided at lateral surface of a substrate having a barrier for making a depletion layer on one surface thereof to thereby increase variation of capacitance without substantially increasing area of the capacitance reading section.

In accordance with the present invention, there is provided a variable capacitor which comprises:

a semiconductive substrate having a barrier for generating a depletion layer on one surface thereof;

a capacitance reading section provided on lateral surface of said semiconductive substrate;

a depletion layer control section provided on the opposite surface of said semiconductive substrate; and a reverse bias means for reversely biasing said depletion layer control section.

Examples of the present invention will now be described with reference to the accompanying drawings, in which:

Fig. 1 is a sectional view showing a prior-art variable capacitor; and

Figs. 2 to 5 are sectional view showing preferred embodiments according to the present invention.

Fig. 2 is a sectional view showing an embodiment according to the present invention in which reference numeral 9 refers to an n^+-type layer, 10 to a p-type layer formed on the n^+-type layer 9, and 11 to a lateral surface of the p-type layer which is θ degrees inclined with respect to the p—n junction 3. Further, reference numeral 12 refers to a depletion layer control electrode provided along the n^+-type layer 9, 13 to capacitance reading section provided on the lateral surface 11 and including a capacitance reading electrode which will be described later. 14 to a common electrode and 15 to an insulative layer.

The capacitance reading section 13 may be formed in a p—n junction configuration by selectively making an n-type region 16 on the lateral surface 11 and providing a capacitance reading electrode 17 along the n-type region 16 as shown in Fig. 3, in an MIS configuration by providing the capacitance reading electrode 17 on the lateral surface 11 along the insulative layer 15 as shown in Fig. 4, or a Schottky junction configuration by providing metal 18 capable of forming a Schottky barrier and for serving as a capacitance reading electrode.

With this arrangement, when reverse bias voltage V_R is applied between the depletion layer control electrode 12 and the common electrode 14, the depletion layer 8 begins to expand from the p—n junction 3 mainly in the p-type layer 10, where impurity concentration is low, in accordance with increase of the reverse bias voltage and the thickness d of the depletion layer 8 increases. At the same time, length D of the depletion layer 8 along the slope A of the lateral surface 11 also increases while length B of the part on the lateral surface 11 where the depletion layer 8 does not invade is gradually reduced.

In other words, when varying reverse bias voltage V_R, the thickness d of the depletion layer 8 expands or contracts to thereby vary the length D thereof along the lateral surface 11. Therefore, the length B along the lateral surface 11 can also be controlled to thereby increase or decrease the area thereof in response to variation of the area of the depletion layer. As the result, capacitance C_1 can be obtained between the capacitance reading electrode 17 or 18 and the p-type layer 10 from the area corresponding to the length B.

Further, between the capacitance reading electrode 17 or 18 and the n^+-type layer 9, there is obtained capacitance C obtained by connecting in series the above-mentioned capacitance C_1 and capacitance C_2 between the upper and lower places of the depletion layer 8 and further connecting in parallel those two capacitances C_1 and C_2 to capacitance C_3 produced between the capacitance reading electrode 17 or 18 and the n^+-type layer 9 through the area corresponding to the above-mentioned length

$$D\ (C=C_3+C_1.C_2/C_1+C_2).$$

Accordingly, there occurs capacitance variation between the capacitance reading electrode 17 or 18 and the common electrode 14 to thereby reduce the length B in accordance with increase of the thickness d of the depletion layer. Therefore, capacitance variation which is read at the capacitance reading section R_1 between the capacitance reading electrode 17 or 18 and the common electrode 14 becomes smaller so that capacitance variation corresponding to variation of the reverse bias voltage can be read. This means that capacitance variation which is read at the capacitance reading section R_1 between the capacitance reading electrode 17 or 18 and the common electrode 14 is controlled by the reverse bias voltage applied between the depletion layer control electrode 12 and the common electrode 14. It should be noted that capacitance which is read at a capacitance reading section R_2 between the capacitance reading electrode 17 or 18 and the depletion layer control electrode12 is also controlled by reverse bias voltage V_R. Further, the capacitance which is read at the capacitance reading electrode 17 or 18 includes capacitance by the insulative layer 15 in addition to that by depletion layer 8.

When assuming the slanting angle of the lateral surface 11 being $\theta°$, the efficient area of the capacitance reading electrode 17 or 18 may be so large as $1/\sin\theta$ times of the horizontal area. Therefore, even if a chip having the same horizontal area is used, larger capacitance variation can be obtained. This means that for obtaining the same capacitance variation, a smaller chip may be used. It is clear that smaller is the angle θ, larger is the efficiency of the present invention. However, θ may be determined suitably case by case.

Such angle θ of the lateral surface 11 can be easily provided by an anisotropic etching method.

Barrier for providing the depletion layer control electrode 12 and producing the depletion layer 8 may be formed in MIS configuration or in Schottky junction configuration instead of the p—n junction configuration adopted in the above-mentioned embodiment.

The variable capacitor with three terminals as described in the above may simultaneously be assembled on manufacturing an IC for an electronic tuning circuit in the front end of an AM radio receiver. This means conventional IC manufacturing process can be used as it is. In the prior art, however, since it has been difficult to simultaneously form a variable capacitor upon manufacturing IC, it has been necessary to connect a variable capacitor as a separately made part to a tuning circuit.

As apparent from the description in the above, the present invention, so arranged to increase capacitance variation without substantially increasing horizontal area of the capacitance reading section by using a semiconductive substrate having a barrier for producing a depletion layer on one surface thereof and providing such capacitance reading section on the lateral surface of the substrate, permits easier increase of capacitance as compared with a case of simply using horizontal depletion layer capacitance by reverse bias voltage. Further, due to the structures of the depletion layer control section and the capacitance reading section having independent three terminals, it is possible to eliminate undesired influence by input signal. Additionally, since the depletion layer capacitance is not determined only the impurity concentration of the semiconductive region, no complicated means for precisely controlling the impurity concentration is needed, resulting in manufacturing IC with good yield.

Claims

1. A variable capacitor which comprises:

a semiconductive substrate having a barrier for generating a depletion layer on one surface thereof;

a capacitance reading section provided on lateral surface of said semiconductive substrate;

a depletion layer control section provided on the opposite surface of said semiconductive substrate; and

a reverse bias means for reversely biasing said depletion layer control section.

2. A variable capacitor of Claim 1 further including a common electrode provided on said one surface of the semiconductive substrate.

3. A variable capacitor of Claim 1 or Claim 2 in which said lateral surface is slanted.

4. A variable capacitor of Claim 1, 2 or 3 further comprising a first capacitance reading terminal provided between said capacitance reading section and said depletion layer control section.

5. A variable capacitor of Claim 1, 2 or 3 which further comprises a second capacitance reading

terminal provided between said capacitance reading section and said common electrode.

6. A variable capacitor of Claim 3, 4 or 5 in which said semiconductive substrate comprises an n^+-type layer and a p-type layer on said n^+-type layer and said slanted lateral surface is made along said p-type layer.

7. A variable capacitor of Claim 1, 2, 3 or 6 in which said capacitance reading section is made in MIS configuration.

8. A variable capacitor of Claim 1, 2, 3 or 6 in which said capacitance reading section is made in p—n junction configuration.

9. A variable capacitor of Claim 1, 2, 3 or 6 in which said capacitance reading section is made in Schottky junction configuration.

10. A variable capacitor substantially as hereinbefore described with reference to and as illustrated in Figures 2 to 5 of the accompanying drawings.

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